UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,283	07/31/2001	Duane E. Galbi	00CXT0725N-1	2490

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EXAMINER
SCHEIBEL, ROBERT C

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/919,283	GALBI ET AL.
	Examiner	Art Unit	
	Robert C. Scheibel	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-21* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments, see pages 4 and 5, and paragraph 3 of page 10, filed 6/21/04, with

respect to objections to the specification have been fully considered and are persuasive. The

objections to the specification have been withdrawn.

2.   Applicant's arguments, see paragraph 4 of page 10, filed 6/21/04, with respect to the

objection to claim 20 have been fully considered and are persuasive. The objection to claim 20

has been withdrawn.

3.   Applicant's arguments, see paragraph 5 of page 10, filed 6/21/04, with respect to the

rejection of claims 16 and 20 under 35 U.S.C. 112, second paragraph have been fully considered

and are persuasive. The rejection of claims 16 and 20 under 35 U.S.C. 112, second paragraph

has been withdrawn.

4.   Applicant's arguments regarding the rejection of claims 1-21 under 35 U.S.C. 103(a), see

the passage from paragraph 6 of page 10 through page 12, filed 6/21/04 have been fully

considered but they are not persuasive.

In paragraph 6 on page 10, applicant restates portions of claim 1. Examiner generally

agrees with this characterization. However, examiner notes that the example of state information

stored in the state information buffers ("a data buffer pointer, a context pointer, a context validity

bit...") is not claimed; thus state information is given a broader interpretation.

In paragraph 7 on page 10, applicant argues that the buffers of Manning are not state

information buffers, but rather are counters. The examiner respectfully disagrees with this

argument. The claims are specified in fairly broad language and the examiner is giving them the

broadest reasonable interpretation. While it is true that some of the state information of Manning are counters, the collective set of information 60-70 of Figure 2 is stored for each link and are state information (see the first sentence of the abstract, for example). A memory buffer is required to store this information and as stated in the previous office action, there are a plurality of such buffers as this state information is stored for each link. Further, as stated in the previous office action, the events are the processing of the packets and the state information of Manning is associated with these events. The Link_Buffer_Counter 62 provides an indication of the number of buffers (the buffers are used to store the packets and thus represent the events as interpreted above) being used and thus discloses the limitation of "an in-use counter indicating the number of events associated with the contents of said buffer". Applicant also argues in paragraph 6 that the buffers of Manning are not in the co-processor. However, the teaching of the buffers is used to modify Daniel and these buffers would be in the co-processor (EDMA) in Daniel, as modified by Manning.

In the first full paragraph of page 11, applicant argues that claims 2-10 are allowable because claim 1 is allowable. The rejection of claim 1 is maintained as stated above and therefore, claims 2-9 are rejected as in the previous office action. In the second full paragraph of page 11, applicant argues that claim 11 is allowable for reasons similar to claim 1; as stated above, examiner believes that claim 11 is not patentable as specified. Similarly, in the third full paragraph of page 11, applicant argues that claims 12-15 are allowable because claim 11 is allowable; however, the rejection of claim 11 is maintained as stated above and thus claims 12-15 are rejected as in the previous office action. In the last 3 paragraphs of page 11, applicant argues that claims 16-21 are patentable because neither Zhou nor Manning disclose state

information buffers with in-use counters. However, as stated above, examiner disagrees with the

argument that Manning fails to disclose state information buffers with in-use counters; for

reasons similar to those argued above, the previous rejection of claims 16-21 is maintained.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3.   Claims **1-4, 7, and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent 6,373,846 to Daniel et al (hereinafter "Daniel") in view of U.S. Patent 5,896,511 to

Manning et al (hereinafter "Manning").

Regarding claims **1 and 11**, Daniel discloses an integrated circuit for processing events

related to communication packets and method of processing events related to communication

packets in an integrated circuit **(ATMCSI/TU 32 of figure 2)**, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication

packets **(APU 36 of figure 2)**, the processing of each packet being an event **(the events in this**

case are the processing done by the APU to issue commands to the EDMA; for example, see

the description of the EDMA_Move command in column 17, lines 5-10) and having

associated data **(Buffer Data A-C of figure 5)** and context information **(VC Descriptor 118 of**

figures 5 and 6); and

a co-processor **(EDMA unit 40 and CBM 68 of figure 2; see also column 13 line 20-21**

"The EDMA unit 40 is effectively a coprocessor under control of the APU").

Daniel does not disclose expressly the co-processor comprising a plurality of state

information buffers or the limitation of each of said state information buffers having an in-use

counter indicating the number of events associated with the contents of said buffer (claims 1 and

11) or the methods of incrementing and decrementing the in-use counter (claim 11).

Manning discloses state information buffers **(the link-level buffer state information 62,**

64, 66, 68, and 70 of figure 2; see lines 55-58 of column 8) each of said state information

buffers having an in-use counter **(LINK_BUFFER_COUNTER 62)** indicating the number of

events associated with the contents of said buffer. Manning also discloses incrementing the in-

use counter associated with said state information buffer when an event is associated with said

state information buffer **(figure 4 – incrementing LINK_BUFFER_COUNTER)** and

decrementing the in-use counter of said state information buffer when said event associated with

said buffer is finished **(figure 5B – decrementing LINK_BUFFER_COUNTER)**.

Daniel and Manning are analogous art because they are from the same field of endeavor

of ATM switching devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel by adding the link level state information of Manning. The motivation for doing so would have been to minimize "the wasting of link bandwidth to transmit flow control update information" as specified in lines 25-26 of column 2 of Manning.

Therefore, it would have been obvious to combine Manning with Daniel for the benefit of minimizing the wasted link bandwidth used for flow control update information to obtain the invention as specified in claims 1 and 11.

Regarding claims **12,** with the features in the parent claim 11 addressed above, Daniel, as modified, discloses the plurality of state information buffers **(the link-level buffer state information 62, 64, 66, 68, and 70 of figure 2; there are a plurality of these buffers because there is one for each link in the system).**

Regarding claims **2, 4, 7, and 14,** with the features in the parent claims 1 and 11 addressed above, Daniel, as modified, discloses the plurality of context buffers **(VC Descriptor 118 of figures 5 and 6),** and the plurality of data buffers for storing data **(the CBM contains a plurality of data buffers – Buffer Data A-C of figure 5).**

Regarding claims **3 and 13,** with the features in the parent claims 1 and 11 addressed above, Manning discloses the in-use counter for the context buffers **(BUFFER_COUNTER 32')** and the incrementing **(Figure 4 – incrementing BUFFER_COUNTER)** and decrementing **(Figure 5A – decrementing BUFFER_COUNTER)** of this counter.

Daniel and Manning are analogous art because they are from the same field of endeavor of ATM switching devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel by adding the per-connection counter BUFFER_COUNTER, and additionally by adding the link level state information of Manning as discussed above. The motivation for doing so would have been to add flow control to Daniel as specified in .

Therefore, it would have been obvious to combine Manning with Daniel for the benefit of minimizing the wasted link bandwidth used for flow control update information to obtain the invention as specified in claims 1 and 11.

4.   Claims **5, 6, 8-9, and 15-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,373,846 to Daniel et al (hereinafter "Daniel") in view of U.S. Patent 5,896,511 to Manning et al (hereinafter "Manning") and in further view of U.S. Patent 6,310,879 to Zhou et al (hereinafter "Zhou").

Regarding claims **16 and 21**, Daniel discloses an integrated circuit **(ATMCSI/TU 32 of figure 2)**, the core processor **(APU 36 of figure 2)**, the co-processor **(EDMA unit 40 and CBM 68 of figure 2; see also column 13 line 20-21 "The EDMA unit 40 is effectively a coprocessor under control of the APU")**, and the data buffers **(Buffer Data A-C of figure 5)**. Regarding claim 21, Daniel further discloses the context buffers **(VC Descriptor 118 of figures 5 and 6)**.

Daniel does not disclose expressly the state information buffers, the in-use counters, or the passing of data between events.

Manning discloses state information buffers **(the link-level buffer state information 62, 64, 66, 68, and 70 of figure 2; see lines 55-58 of column 8)** each of said state information buffers having an in-use counter **(LINK_BUFFER_COUNTER 62)**.

Daniel and Manning are analogous art because they are from the same field of endeavor of ATM switching devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Daniel by adding the link level state information of Manning. The motivation for doing so would have been to minimize "the wasting of link bandwidth to transmit flow control update information" as specified in lines 25-26 of column 2 of Manning.

Daniel and Manning, as combined, fail to disclose an in-use counter for the data buffers or the passing of data between events.

Zhou discloses the use of a counter with a data buffer **(the count 24 described in column 6, lines 35-36 "Preferably, the cell 14 includes a count 24 which identifies all ports 18 the cell 14 will be sent out")**. In addition, Zhou discloses passing the data buffer between multiple ports. The data buffer is effectively passed to another port for transmission to another multicast destination each time the count is decremented.

Daniel and Manning and Zhou are analogous art because they are from the same field of endeavor of ATM switching devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply an in-use count to the data buffers of Daniel, as modified, and to allow the decrementing of this count to effectively indicate the passing of the data buffer to another port.

The suggestion/motivation for doing so would have been to allow Daniel, as modified, to support multicasting while utilizing as little memory as possible. This is suggested by Zhou in column 1, lines 29-32 "Ideally, as little memory as possible should be utilized to maintain the

cell for all the different locations to which it will be sent. The present invention provides an

efficient approach to providing a cell to a multiplicity of connections for multicast.".

Therefore, it would have been obvious to combine Zhou with Daniel and Manning for the

benefit of providing an efficient method of supporting multicast to obtain the invention as

specified in claims 16 and 21.

Regarding claims **5, 8, and 9**, with the features of the parent claims 1 and 7 addressed

above, Zhou teaches an in-use counter for the data buffers **(the count 24 described in column 6,**

lines 35-36). Manning discloses the in-use counter for the context buffers

(BUFFER_COUNTER 32').

Regarding claim **6**, with the features of the parent claim 1 addressed above, Zhou

discloses passing the data buffer between multiple ports. The data buffer is effectively passed to

another port for transmission to another multicast destination each time the count 24 is

decremented.

Regarding claims **15 and 20**, with the features of the parent claims 11 and 16 addressed

above, Manning teaches incrementing the in-use counter associated with said state information

buffer **(figure 4 – incrementing LINK_BUFFER_COUNTER)** and decrementing the in-use

counter of said state information buffer **(figure 5B – decrementing**

LINK_BUFFER_COUNTER). Manning also teaches the incrementing **(Figure 4 –**

incrementing BUFFER_COUNTER) and decrementing **(Figure 5A – decrementing**

BUFFER_COUNTER) of the in-use counter associated with the context buffer. Zhou teaches

incrementing **(column 7, lines 45-47 "Cell C2 has its count 24 incremented to 2 since there**

are two ports, port 1 and port N which cell C2 will go out.") and decrementing **(column 6,**

lines 44-47 **"The removing step can include the step of decrementing by one a value of the count 24 equal to the number of ports 18 the cell 14 will be sent out."**) the counter associated with the data buffer.

Regarding claim **17**, with the features of the parent claim 16 addressed above, Daniel, as modified, discloses context information buffers **(VC Descriptor 118 of figures 5 and 6)**.

Regarding claim **18**, with the features of the parent claim 17 addressed above, Manning discloses the in-use counter for the context buffers **(BUFFER_COUNTER 32')**.

Regarding claim **19**, with the features of the parent claim 16 addressed above, Daniel, as modified teaches a plurality of data buffers **(Buffer Data A-C of figure 5)**, and Manning teaches a plurality of state information buffers **(the link-level buffer state information 62, 64, 66, 68, and 70 of figure 2; see lines 55-58 of column 8; one per link)**.

Daniel and Manning and Zhou are analogous art because they are from the same field of endeavor of ATM switching devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply an in-use count to the data buffers of Daniel, as modified, and to allow the decrementing of this count to effectively indicate the passing of the data buffer to another port.

The suggestion/motivation for doing so would have been to allow Daniel, as modified, to support multicasting while utilizing as little memory as possible. This is suggested by Zhou in column 1, lines 29-32 "Ideally, as little memory as possible should be utilized to maintain the cell for all the different locations to which it will be sent. The present invention provides an efficient approach to providing a cell to a multiplicity of connections for multicast.".

Therefore, it would have been obvious to combine Zhou with Daniel and Manning for the

benefit of providing an efficient method of supporting multicast to obtain the invention as

specified in claims 5, 6, 8-9, and 15, 17-20.

Allowable Subject Matter

5.   Claim **10** is objected to as being dependent upon a rejected base claim, but would be

allowable if rewritten in independent form including all of the limitations of the base claim and

any intervening claims.

Conclusion

6.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169.

The examiner can normally be reached on Monday and Thursday from 6:30-5:00 Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RCS   9-23-04
Robert C. Scheibel
Examiner
Art Unit 2666

DWGTON
PRIMARY EXAMINER